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Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on ER 408659660 US

11/19/03
(Date of Deposit)

Karen Cinq-Mars
Karen Cinq-Mars (Signature)

11/19/03
(Date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of : November 19, 2003
Neves et al. :
Serial No. : Examiner:
Filed: Herewith : IBM Corporation
Dept. 18G/Bldg. 300-482
2070 Route 52
Hopewell Junction,
New York 12533-6531
Title: A METHOD TO IDENTIFY
GEOMETRICALLY NON-OVERLAPPING
OPTIMIZATION PARTITIONS FOR
PARALLEL TIMING CLOSURE :

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56 and in accordance with the practice under 37 C.F.R. §§ 1.97 and 1.98, the Examiner's attention is directed to the document listed on the enclosed Form PTO-1449. A copy of the listed document is also enclosed.

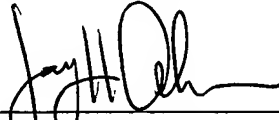
It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed Form PTO-1449 be returned indicating that such information has been considered.

FIS920030387US1

Applicants' undersigned attorney may be reached by telephone at (845) 894-3667.

All correspondence should continue to be directed to the below listed address.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Jay M. Anderson", written over a horizontal line.

Jay M. Anderson
Attorney for Applicants
Registration No.38,371

INTERNATIONAL BUSINESS MACHINES CORPORATION
Intellectual Property Law Department
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INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>	Docket Number (Optional) FIS920030387US1	Application Number
	Applicant(s) Neves et al.	
	Filing Date	Group Art Unit

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		"Multi-objective circuit partitioning for cutsize and path-based delay minimization", Ababei et al., 2002 IEEE, ppgs. 181-185

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.